This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) An integrated circuit (IC) comprising:
   a universal bus;
   a central processing unit (CPU) coupled to the universal bus; and
   a program control unit (PCU) comprising at least one program control register coupled to the universal bus for receiving control signals via the universal bus only.

2. (original) The IC of claim 1 further comprising a plurality of CPUs coupled to the universal bus.

3. (original) The IC of claim 1 further comprising a plurality of peripheral devices coupled to the universal bus.

4. (original) The IC of claim 3 wherein the plurality of peripheral devices are selected from the group consisting of: PCUs, Arithmetic Logic Units (ALUs), Cyclic Redundancy Checkers (CRCs), Data Encryption Standard (DES) engines, data transceivers, Secure Memory Units (SMUs), Memory Mapping Units (MMUs), Data registers, Data stores, and other memory storage devices.

5. (original) The IC of claim 2 wherein at least one of the plurality of CPUs controls the universal bus at a moment in time.

6. (original) The IC of claim 3 wherein the plurality of peripheral devices are slaved to the universal bus.

7. (currently amended) The IC of claim 1 wherein the PCU has at least one instruction set and the CPU has at least one instruction set.

8. (canceled)

9. (original) The IC of claim 7 wherein the at least one PCU instruction set is stored separately from the at least one CPU instruction set.

10. (original) The IC of claim 9 wherein the PCU instruction set can be altered without altering the CPU instruction set.

11. (currently amended) An application specific integrated circuit (ASIC) comprising:

a universal bus;

a central processing unit (CPU) coupled to the universal bus; and

a program control unit (PCU) comprising at least one program control register coupled to the universal bus,

wherein, the CPU is coupled to the PCU without dedicated control lines.

12. (original) The ASIC of claim 11 further comprising a memory mapping unit (MMU) slaved to the universal bus, said MMU translates logical addresses used by the CPU to physical addresses.

13. (original) The ASIC of claim 11 wherein the CPU communicates with the PCU by way of the universal bus only.

14. (currently amended) A micro controller comprising:

a universal bus having physical address lines;

a central processing unit (CPU) having an instruction set and employing logical addressing, coupled to the bus; and

a program control unit (PCU) having an instruction set and comprising at least one program control register, coupled to the universal bus for receiving control signals from the bus only,

wherein, the CPU is coupled to the PCU without dedicated control lines.

15. (original) The micro controller of claim 14 wherein the PCU instruction set is stored separately from CPU instruction set.

16. (original) The micro controller of claim 14 wherein the PCU instruction set can be altered without altering the CPU instruction set.

17. (currently amended) An application specific computing device having an IC, said IC comprising:

a universal bus;

a central processing unit (CPU) coupled to the universal bus; and

a program control unit (PCU) comprising at least one program control register coupled to the universal bus for receiving control signals via the universal bus only.

18. (original) The device of claim 17 wherein the PCU has an instruction set and the CPU has an instruction set, the PCU instruction set being stored and maintained separately from the CPU instruction set.

19. (original) The device of claim 18 wherein the PCU instruction set can be altered without altering the CPU instruction set.

20. (original) The device of claim 17 wherein the CPU is coupled to the PCU without dedicated control lines.

21. (original) The IC of claim 17 further comprising a plurality of CPUs coupled to the universal bus.

22. (original) The IC of claim 17 further comprising a plurality of peripheral devices coupled to the universal bus.

23. (original) The device of claim 17 being selected from the group of devices consisting of smartcards, calculators, personal organizers, personal communicators, consumer electronic devices, home and office equipment/appliances, readers/scanners, wireless control units, and the combinations thereof.

24. (currently amended) An integrated circuit (IC) comprising:

a universal bus having physical address lines with associated physical addresses;

a central processing unit (CPU) that employs logical addressing and is coupled to the universal bus;

a program control unit (PCU) comprising at least one program control register coupled to the universal bus; and

a memory mapping unit (MMU) slaved to the universal bus

wherein the MMU translates logical addresses used by the CPU to physical addresses associated with the universal bus.

25. (new) The IC of claim 1 further comprising a memory module coupled to the PCU via a memory bus.

26. (new) The ASIC of claim 11 further comprising a memory module coupled to the PCU via a memory bus.

27. (new) The micro controller of claim 14 further comprising a memory module coupled to the PCU via a memory bus.

28. (new) The IC of claim 17 further comprising a memory module coupled to the PCU via a memory bus.